IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

translating a design description into configurations for a plurality of processing elements on a single integrated circuit; ~~and~~

setting at least one packet size for packet communications between the plurality of processing elements on the single integrated circuit[[.]];

profiling a design represented by the configurations for the plurality of processing elements; and

changing a power supply voltage value in response to the profiling.

2. (Original) The method of claim 1 wherein translating comprises partitioning the design into a plurality of functions.

3. (Original) The method of claim 2 wherein translating further comprises compiling the plurality of functions to code to run on at least one of the plurality of processing elements.

4. (Canceled)

5. (Canceled)

6. (Currently Amended) The method of claim [[4]] 1 further comprising changing a clock frequency in response to the profiling.

7. (Currently Amended) The method of claim [[4]] 1 further comprising changing the at least one packet size in response to the profiling.

8. (Currently Amended) The method of claim [[4]] 1 wherein profiling produces information describing latency.

9. (Currently Amended) The method of claim [[4]] 1 wherein profiling produces information describing throughput.

10. (Currently Amended) The method of claim [[4]] 1 further comprising comparing user constraints with output from the profiling.

11. (Original) The method of claim 10 wherein the user constraints include latency.

12. (Original) The method of claim 10 wherein the user constraints include throughput.

13. (Currently Amended) The method of claim [[4]] 1 further comprising modifying parameters of the processing elements in response to the profiling.

14. (Currently Amended) A method comprising:

dividing a design description into a plurality of functions;

compiling at least one function into machine code to run on a first processing element;

translating at least one other function into a configuration for a second processing element; ~~and~~

setting a packet size for packet communications between the first and second processing elements[[.]];

profiling a design with the configuration packets; and

modifying a power supply voltage of the first processing element in response to the profiling.

15. (Original) The method of claim 14 further comprising generating configuration packets to configure an integrated circuit that includes the first and second processing elements.

16. (Original) The method of claim 15 further comprising configuring the integrated circuit with the configuration packets.

17. (Original) The method of claim 14 wherein translating at least one other function comprises translating a plurality of other functions into a configuration for the second processing element.

18. (Canceled)

19. (Currently Amended) The method of claim ~~18~~ 14 further comprising modifying the packet size in response to the profiling.

20. (Canceled)

21. (Currently Amended) The method of claim ~~18~~ 14 further comprising modifying a power supply voltage of the second processing element in response to the profiling.

22. (Currently Amended) The method of claim ~~18~~ 14 further comprising modifying a clock frequency of the first processing element in response to the profiling.

23. (Currently Amended) The method of claim ~~18~~ 14 further comprising modifying a clock frequency of the second processing element in response to the profiling.

24. (Currently Amended) An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine performing:

reading a design description;

compiling the design description to configure a plurality of processing elements; ~~and~~

determining a packet size for communications between at least two of the plurality of processing elements[[.]];

profiling the design; and

modifying a power supply voltage of at least one of the plurality of processing elements in response to the profiling.

25. (Canceled)

26. (Currently Amended) The apparatus of claim ~~25 wherein modifying at least one parameter comprises~~ 24 further comprising modifying a clock rate of at least one of the plurality of processing elements in response to the profiling.

27. (Currently Amended) The apparatus of claim ~~25 wherein modifying at least one parameter comprises~~ 24 further comprising modifying the packet size in response to the profiling.

28. (Currently Amended) An electronic system comprising:

a processing element; and

a static random access memory to hold instructions that when accessed result in the processing element performing reading a design description, compiling the design description to configure a plurality of processing elements, ~~and~~ determining a packet size for communications between at least two of the plurality of processing elements[[.]]; profiling the design, and modifying a power supply voltage of at least one of the plurality of processing elements in response to the profiling.

29. (Canceled)

30. (Currently Amended) The electronic system of claim ~~29 wherein modifying at least one parameter comprises~~ further comprising modifying the packet size in response to the profiling.